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[VARIABLE SIGMA ADJUST METHODOLOGY FOR STATIC TIMING]

Abstract

The invention presents a method of accommodating for across chip line variation (ACLV) and/or changing static timing of an integrated circuit design. The invention first establishes a circuit design having initial timing requirements and an initial voltage supply and also establishes a relationship between gate timing variations caused by voltage supply changes and gate timing variations caused by manufacturing processing changes. Then, according to the customer's orders that change the initial timing requirements to revised timing requirements, the invention changes the initial voltage supply to a revised voltage supply to accommodate the revised timing requirements (and ACLV if desired) based on the relationship between voltage limits and transistor delay. This process of changing the initial voltage supply does not alter the circuit design.